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A Comparative Study Of Low Power Consumption Techniques In A VLSI Circuit

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ABSTRACT
Power optimization has become an important factor in designing a VLSI circuit. Earlier dynamic power was single largest concern but as transistor size decreases static power dominates the dynamic power. A comparable analysis of different low power, leakage current reduction techniques like sleep, stack, sleepy keeper and reverse body bias with sleep and stack has been done. Based on simulations performed on a XNOR circuit, the reverse body with sleep and stack achieves up to 60% less power consumption as compared to the base case which is better than other conventional techniques. Simulations to estimate power consumption are done on a TANNER EDA tool at 90 nm technology.
Keywords – Leakage current reduction, Power optimization, Sleep, Sleepy keeper, Stack.

I.   INTRODUCTION
With advancement in VLSI we require devices with less power consumption and short delay. But in actual these both are contradictory to each other. As supply voltage is scaled down to reduce power dissipation, threshold voltage is also scaled down to maintain performance. So from view point of performance, it is essential to have smaller threshold voltage but sub threshold current which is one of the leakage current component increases linearly as we reduce the threshold voltage.

Leakage power dissipation is becoming one of the most challenging issue in designing low power VLSI circuits. Overviews of various techniques like sleep, stack, etc for leakage power reduction has been discussed in paper. The need for designing low power vlsi chips has become very important as we know the device dimension is getting reduced so more number of transistors are being packed onto a chip Thus resulting in increased power dissipation. So various techniques like Sleep, Stack, Sleepy keeper etc. have been proposed to overcome this problem of increased power dissipation.

II.   LITERATURE SURVEY
M. Geetha Priya et al. have done comprehensive study and analysis of various leakage power minimization techniques in 2012. Their research study is mainly focused on circuit performance parameters. It has been implied from the current literature that only an appropriate choice of leakage power minimization technique for a specific application can be effectively carried by a VLSI circuit designer based on sequential analytical approach. [1]

K. Ghana Deepika *et al.* presented Sleepy Keeper Approach for Power Performance Tuning in VLSI Design and various techniques like Sleep technique, Stack technique etc. that are used to reduce leakage power and talked about the disadvantages of each technique which limit the applications of each technique. Further, they have introduced sleepy keeper approach which can be used to reduce the power dissipation of the circuit in idle state while maintaining logic. Multi threshold transistors are used in order to reduce sub threshold leakage power and also to increase the switching speed of the circuit. [2]

III.   METHODOLOGY
All the simulations are done on XNOR gate circuit at 90nm technology. The proposed techniques are discussed below:
3.1   SLEEP TRANSISTOR APPROACH
In this technique, high threshold voltage PMOS transistor is connected between Vdd and pull up network of the circuit and NMOS transistor is connected between ground and pull down network. As high threshold voltage transistor have lower sub threshold current. Thus this technique reduces leakage power effectively. It operates in two modes Sleep and Active mode.[3] In case of sleep mode sleep transistors are turned off thus gating the supply voltage. By cutting off the power supply this can reduce the leakage power. In active mode the sleep transistors are on, this provides charging and discharging path to output during any change in input. Disadvantage of this technique is that it does not hold state, it destructs the state and thus there is problem of floating output voltage.
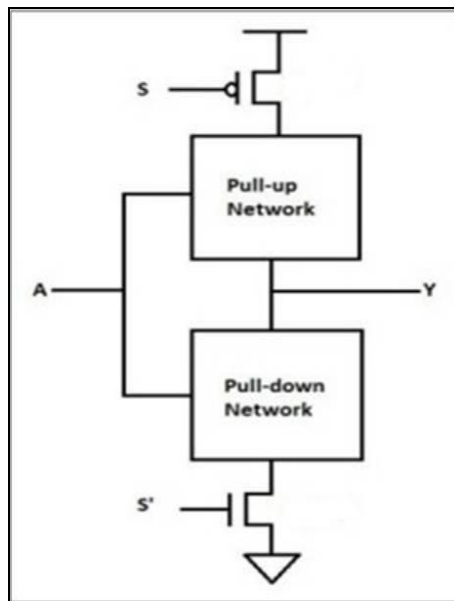
Figure1. Sleep transistor technique

3.2 STACK APPROACH

This technique divides the transistor into two half size transistors. When more than one transistor in series is turned off, the leakage current has strong dependence on number of turned off transistor. Due to exponential dependence of sub threshold current on gate source voltage, leakage current is reduced because of negative gate to source voltage. However there is degradation in performance.[4]
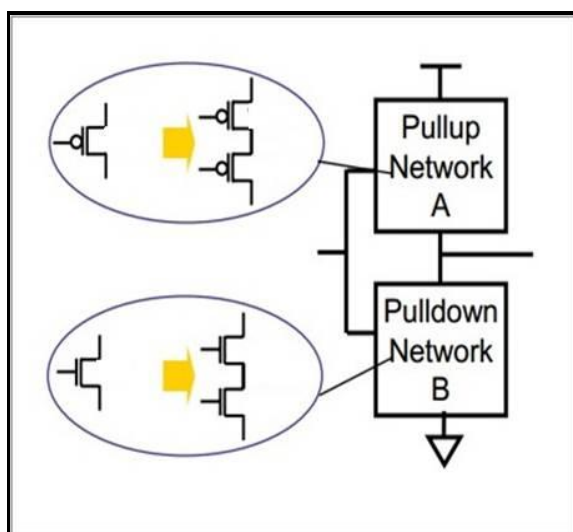

Figure2. Stack approach

3.3 SLEEPY KEEPER APPROACH

To overcome the disadvantage of sleep approach of destructive output sleepy keeper approach uses two additional transistors to maintain logic state during sleep mode and the two transistors are driven by the output of the circuit implemented. In this additonal NMOS transistor is placed parallel to PMOS sleep transistor between Vdd and pull up network and an additional PMOS transistor is placed parallel to NMOS sleep transistor between pull down network and ground.[5][6] When sleep transistors are turned off, in order to maintain the output logic, suppose '1', the additional NMOS transistor placed in parallel to PMOS sleep transistor will be only source to VDD. Thus, the output logic is maintained when circuit switches from sleep mode to active mode.
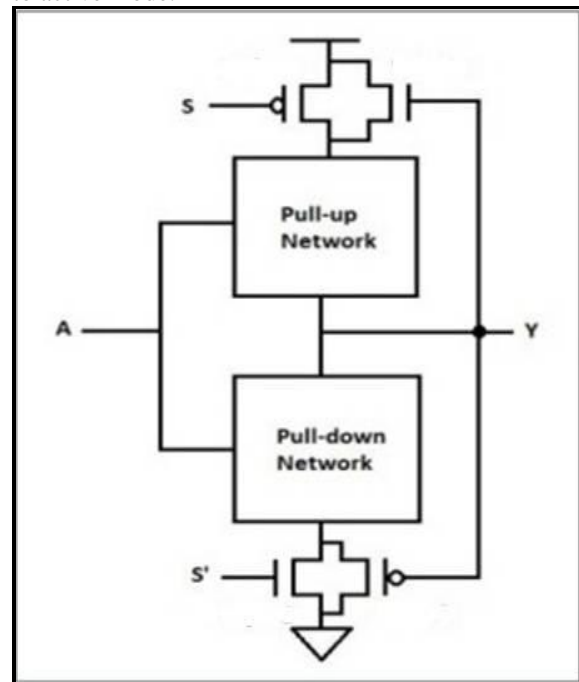

Figure3. Sleepy keeper approach

IV. PROPOSED TECHNIQUE (REVERSE BODY BIAS WITH SLEEP AND STACK)

In this technique sleep approach and stack approach, both are combined together with reverse body biasing in pull down network. Reverse body biasing increases the threshold voltage and thus sub threshold current is reduced. As we know there is tradeoff between power and delay we obtain maximum reduction in power and delay as compared to previously discussed techniques. This technique is the most efficient technique.
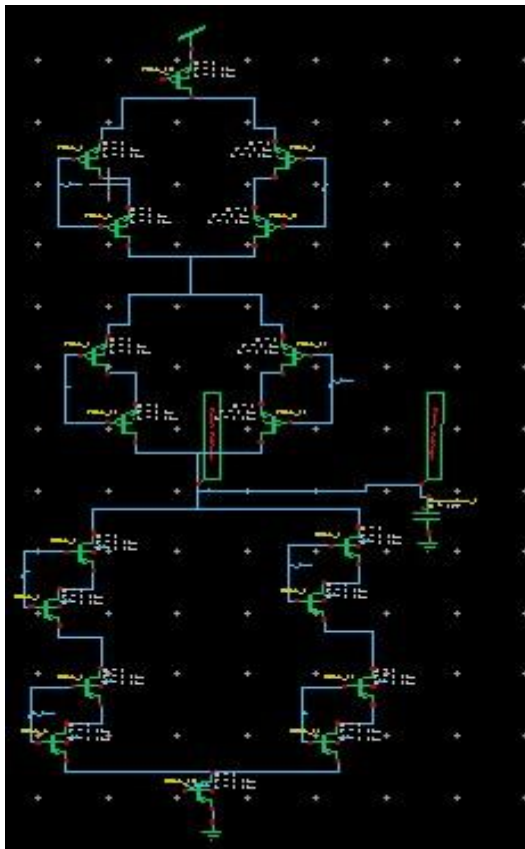
Active Power (10^-6)	NA	7.4135	7.7418	NA	4.4547
Delay (s)	8.4339 *10^-11	5.3197 *10^-10	6.1645 *10^-10	8.4012 *10^-10	4.8254 *10^-10

Table1. Result obtained by using different techniques and their comparative analysis.

As seen from the above table, it can be concluded that according to our simulations, proposed technique gave the best results with maximum reduction in power and best power delay trade off.

	Reduction of Average Power from normal XNOR
Sleep	40.98%
Keeper	39.93%
Stack	18.11%
Proposed	63.41%

Table 2. percentage reduction in average power
Percentage reduction in power obtained from reverse body bias with stack and sleep is observed to be maximum.
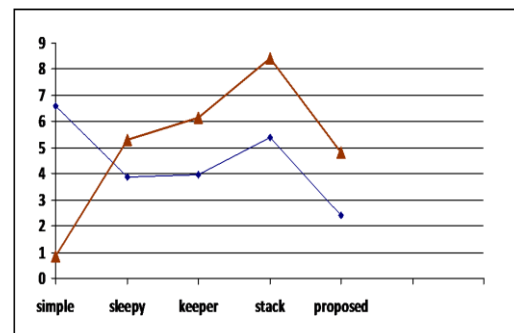

Figure4. Reverse body bias with sleep and stack technique implemented on XNOR circuit.

V. RESULTS AND DISCUSSION

According to our simulations performed on xnor gate circuit we obtained maximum reduction in power using proposed technique. The simulation are carried out at 1.8 V supply voltage. The circuit is designed using low threshold voltage of 0.2 V and high threshold voltage sleep transistors of 0.4 V in sleep, sleepy keeper and reverse body bias with sleep and stack techniques.

	Simple (W)	Sleepy (W)	Keeper (W)	Stack (W)	Proposed (W)
Avg Power (10^-6)	6.5765	3.8810	3.9502	5.3851	2.4061
Sleep Power (10^-6)	NA	0.34848	0.15871	NA	0.3574

Figure5. X axis: Techniques, Y axis: Average power (Blue) in 10^-6 W and Delay (Red) in 10^-10 (S)

VI.   CONCLUSION

The proposed XNOR gate circuit has been designed   and simulated on Tanner EDA tool version 14.11 at 90 nm technology and 1.8 v supply voltage.   Though we obtained decrease in power in sleep approach than base circuit but there is destruction of state. In case of stack approach there is large performance degradation as compared to other techniques. As we know there is tradeoff between power and delay, reverse body bias with sleep and stack approach results in maximum reduction with smallest delay while simultaneously preserving precise logic state in sleep mode. Thus proposed technique shows more than 60% power reduction as compared to normal XNOR circuit. So, good results were obtained from proposed technique. The proposed technique provides efficient method to reduce power. In future research can be done to propose techniques to reduce power consumption without compromise in performance.

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